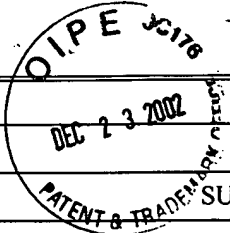


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		Atty Docket No.	Serial No.	
		M-799-4C US	08/851,608	
SUMMARY OF CITED DOCUMENTS		Applicants: Bulucea et al.		
		Filing Date	Group	
		5 May 1997	2811	
U.S. Patent Documents				
Document Number	Date	Name	Class	Subclass
3,412,297	11/19/68	Amlinger	317	235
3,924,265	12/2/75	Rodgers	357	23
4,145,700	03/20/79	Jambotkar	357	23
4,148,047	04/03/79	Hendrickson	357	23
4,345,265	08/17/82	Blanchard	357	23
4,364,074	12/14/82	Garnache et al.	357	23
4,374,455	02/22/83	Goodman	29	571
4,376,286	03/08/83	Lidow et al.	357	23
4,398,339	08/16/83	Blanchard et al.	29	571
4,420,379	12/13/83	Tonnel	204	38
4,443,931	04/24/84	Baliga et al.	29	571
4,506,435	03/26/85	Pliskin et al.	29	576
4,532,534	07/30/85	Ford et al.	357	23.4
4,593,302	06/03/86	Lidow et al.	357	23.4
4,631,564	12/23/86	Neilson et al.	357	23.4
4,663,644	05/05/87	Shimizu	357	23.14
4,680,853	07/21/87	Lidow et al.	29	571
4,764,481	08/16/88	Alvi et al.	437	56
4,767,722	08/30/88	Blanchard	437	41
4,783,694	11/08/88	Merrill et al.	357	51
4,794,561	12/27/88	Hsu	365	182
4,808,543	02/28/89	Parrillo et al.	437	38
4,824,793	04/25/89	Richardson et al.	437	47
4,893,160	01/09/90	Blanchard	357	23.4
4,914,058	04/03/90	Blanchard	437	203
4,983,535	01/08/91	Blanchard	437	40
5,016,068	05/14/91	Mori	357	23.5
5,019,522	05/28/91	Meyer et al.	437	29
5,034,785	07/23/91	Blanchard	357	23.4
5,160,491	11/03/92	Mori	437	40

CRANE

3/03

## Foreign Patent Documents

Class subclass

DIPE JC178  
DEC 23 2002  
SWC  
PATENT & TRADEMARK OFFICE

Document	Date	Country	Class subclass
54-57871	05/10/79	Japan	
55-146976	11/15/80	Japan	
57-18365	01/30/82	Japan	
57-72365	05/06/82	Japan	
58-137254	08/15/83	Japan	
59-80970	05/10/84	Japan	
59-181668	10/16/84	Japan	
59-193064	11/01/84	Japan	
60-28271	02/13/85	Japan	
62-12167	01/21/87	Japan	
62-16572	01/24/87	Japan	
62-37965	02/18/87	Japan	
63-114173	05/19/88	Japan	
63-124762	08/15/88	Japan	
63-224260	09/19/88	Japan	
DE 3028561 A1	02/18/82	Germany	

SWC

## OTHER ART

Blanchard, "Optimization of Discrete High Power MOS Transistors", Ph.D. dissertation, Stanford Univ., December 1981, copyright 1982, pp. I - XIV and 1 - 195.

Bulucea, "Avalanche Injection Into the Oxide in Silicon Gate-Controlled Devices I. Theory," Solid-State Electronics, Vol. 18, 1975, pgs. 363 - 374.

Bulucea, "Avalanche Injection into the Oxide in Silicon Gate-Controlled Devices II. Experimental Results," Solid-State Electronics, Vol. 18, 1975, pgs. 381 - 391.

Chang et al., "Self-aligned UMOSFET's With A Specific On-Resistance of  $1 \text{ m}\Omega \cdot \text{cm}^2$ ," IEEE Trans. Electron Devices, Vol. ED-34, 1987, pgs. 2329 - 2334.

Kato et al., "A Study for High Voltage V-MOS Structure", IEICE Trans. C, Vol. 81, No. 7, ED 81 - 4, 1981, pgs. 25 - 32.

Kato et al., "Design of New Structural High Breakdown Voltage V-MOSFET--Static Shield V-MOSFET", Elec. and Comms. in Japan, Vol. 66-C, No. 6, 1983, pgs. 95 - 105 for English version, pgs. 462 - 469 for Japanese version.

Kato et al., "Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect", Review Elec. Coms. Labs., Vol. 32, No. 6, 1984, pgs. 1107 - 1114 for English version, Vol. 33, No. 2, 1984, pgs. 257 - 268 for Japanese version.

Lisiak et al., "Optimization of Nonplanar Power MOS Transistors," IEEE Trans. Electron Devices, October 1978, pgs. 1229 - 1234.

Marcus et al., "The Oxidation of Shaped Silicon Surfaces," Journal Electrochemical Society: SOLID-STATE SCIENCE AND TECHNOLOGY, Vol. 129, 1982, pgs. 1278 - 1282.

CRANE

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## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Cont'd

5.25  
Suzuki et al., "Device Electronics for Integrated Circuits (John Wiley & Sons), 1977, pgs. 128-137.

Pelly et al., "Applying International Rectifier's HEXFET® Power MOSFETs", HEXFET Databook, Power MOSFET Application and Product Data (3d ed., International Rectifier), Appln. Note 930A, 1985, printed September 1984, pgs. A-11 to A-20.

Pelly, "The Do's and Don'ts of Using Power HEXTFET®s", HEXFET Databook, Power MOSFET Application and Product Data (3d ed., International Rectifier), Appln. Note 936, 1985, printed September 1984, pgs. A-21 to A-26.

Sun, "Physics and Technology of Power MOSFETS", Technical Report IDEZ696-1, Integrated Circs. Lab., Stanford Univ., February 1952, pgs. 100 - 106.

Sun et al., "Modeling of the On-Resistance of LDMOS, VDOS, and VDMOS Power Transistors," IEEE Trans. Electron Devices, February 1980, pgs. 356 - 367.

Sze, Semiconductor Devices, Physics and Technology (John Wiley & Sons), 1985, pg. 401.

Ueda et al., "High Speed Power MOSFET, U-MOS Power Fet", National Technical Report, Vol. 29, No. 2, April 1983, pgs. 1 - 16 for English version, Vol. 29, No. 2, April 1983, pgs. 335 - 342 or 143 - 150 for Japanese version.

Ueda et al., "A New Vertical Power MOSFET Structure With Extremely Reduced On-resistance," IEEE Trans. Electron Devices, January 1985, pgs. 2 - 6.

Wilson et al., "Oxidation of Curved Silicon Surfaces," Journal Electrochemical Society: SOLID-STATE SCIENCE AND TECHNOLOGY, Vol. 134, 1987, pgs. 481- 490.

SW  
Yamabe et al., "Nonplanar Oxidation and Reduction of Oxide Leakage Currents at Silicon Corners by Round-off Oxidation," IEEE Trans. Electron Devices, August 1987, pgs. 1681 - 1687

CRANE

3/03

OIP E JC176  
DEC 23 2002  
PATENT & TRADEMARK OFFICE

#42  
Sheet 1 of 2

U.S. Department of Commerce, Patent and Trademark Office						Atty Docket No.		Serial No.	
						M-799-4C US		08/851,608	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT						Applicants: Bulucea et al.			
(Use several sheets if necessary)									
						Filing Date		Group	
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U.S. Patent Documents									
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
SWC	AA	3,412,297	Nov. 19, 1968	Amlinger	317	235			
	AB	3,924,265	Dec. 2, 1975	Rodgers	357	23			
	AC	4,364,074	Dec. 14, 1982	Garnache et al.	357	23			
	AD	4,374,455	Feb. 22, 1983	Goodman	29	571			
	AE	4,443,931	Apr. 24, 1984	Baliga et al.	29	571			
	AF	4,532,534	Jul. 30, 1985	Ford et al.	357	23.4			
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Foreign Patent Documents									
							Translation		
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SWC	AH	54-57871	05/10/79	Japan			X		
	AI	55-146976	11/15/80	Japan			X		
	AJ	57-18365	01/30/82	Japan			X		
	AK	57-72365	05/06/82	Japan			X		
	AL	58-137254	08/15/83	Japan			X		
	AM	59-80970	05/10/84	Japan			X		
	AN	59-181668	10/16/84	Japan			X		
	AO	59-193064	11/01/84	Japan			X		
	AP	60-28271	02/13/85	Japan			X		
	AQ	62-12167	01/21/87	Japan			X		
	AR	62-16572	01/24/87	Japan			X		
	AS	62-37965	02/18/87	Japan				X	
	AT	63-114173	05/19/88	Japan				X	
	AU	63-124762	08/15/88	Japan			X		
SWC	AV	63-224260	09/19/88	Japan			X		
Examiner		CRANE		Date Considered		3/03			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.									

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(Use several sheets if necessary)

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2811

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SWC	BA	Blanchard, "Optimization of Discrete High Power MOS Transistors", Ph.D. dissertation, Stanford Univ., December 1981, copyright 1982, pp. I - XIV and 1 - 195.	
	BB	Kato et al., "A Study for High Voltage V-MOS Structure", <u>IEICE Trans. C</u> , Vol. 81, No. 7, ED 81 - 4, 1981, pgs. 25 - 32.	
	BC	Kato et al., "Design of New Structural High Breakdown Voltage V-MOSFET--Static Shield V-MOSFET", <u>Elec. and Comms. in Japan</u> , Vol. 66-C, No. 6, 1983, pgs. 95 - 105 for English version, pgs. 462 - 469 for Japanese version.	
	BD	Kato et al., "Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect", <u>Review Elec. Coms. Labs.</u> , Vol. 32, No. 6, 1984, pgs. 1107 - 1114 for English version, Vol. 33, No. 2, 1984, pgs. 257 - 268 for Japanese version.	
	BE	Muller et al., <u>Device Electronics for Integrated Circuits</u> (John Wiley & Sons), 1977, pgs. 128-137.	
	BF	Pelly et al., "Applying International Rectifier's HEXFET® Power MOSFETs", <u>HEXFET Databook, Power MOSFET Application and Product Data</u> (3d ed., International Rectifier), Appln. Note 930A, 1985, printed September 1984, pgs. A-11 to A-20.	
	BG	Pelly, "The Do's and Don'ts of Using Power HEXFET®s", <u>HEXFET Databook, Power MOSFET Application and Product Data</u> (3d ed., International Rectifier), Appln. Note 936, 1985, printed September 1984, pgs. A-21 to A-26.	
	BH	Sun, "Physics and Technology of Power MOSFETS", Technical Report IDEZ696-1, Integrated Circs. Lab., Stanford Univ., February 1982, pgs. 100 - 106.	
	BI	Sun et al., "Modeling of the On-Resistance of LDMOS, VDMOS, and VMOS Power Transistors," <u>IEEE Trans. Electron Devices</u> , February 1980, pgs. 356 - 367.	
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	BM		
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